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Evidence of the ferroelectric polarization in charge transport through WTe_2 Weyl semimetal surface

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Recently, three-dimensional WTe_2 single crystals were found to demonstrate coexistence of metallic conductivity and ferroelectricity at room temperature [1]. The latter usually belongs to the insulators [2–6], but it occurs in WTe_2 due to the strong anisotropy of the non-centrosymmetric crystal structure. The spontaneous polarization of ferroelectric domains is found to be bistable, it can be affected by high external electric field [1]. Scattering of the charge carriers on the domain walls is known to provide noticeable contribution to the sample resistance [7]. Thus, coexistence of metallic and ferroelectric properties should produce new physical effects [8] for electron transport in TMDCs, and, therefore, it should be important for nanoelectronic applications.

The single-crystal flakes of WTe_2 are obtained by regular mechanical exfoliation, also known as scotch-tape technique. Next, the exfoliated samples were transferred on the insulating SiO_2 substrate. While we need thick three-dimensional flakes to preserve WTe_2 semimetal properties, we use two different techniques for Ohmic contacts fabrication for the flakes of different thickness.

For the thinnest, 300–600 nm flakes, the Au leads are defined over the flake surface by standard photolithography and lift-off technique after thermal evaporation of 70 nm Au, see the AFM image in Fig. 1. As usual, thin flakes are about 10–30 μm in the lateral size, so only two or three Au leads can be placed over the flake to form Ohmic contacts with 5 μm distance. These samples are mostly suitable for the two-point transport measurements.

The thicker (1–3 μm) flakes are about 100 μm in lateral size, which allows different multiple contact geometries. However, standard 70–100 nm thick Au leads can not be formed across the 1–3 μm step, so we use different contact technique. Thick flakes are transferred to SiO_2 substrate with pre-defined Au leads pattern, the flake is slightly pressed to the leads by another oxidized silicon substrate. This procedure has been verified to provide electrically stable contacts with high quality interfaces. Also, WTe_2 surface with Au contacts is protected from any contamination by SiO_2 substrate in this case.

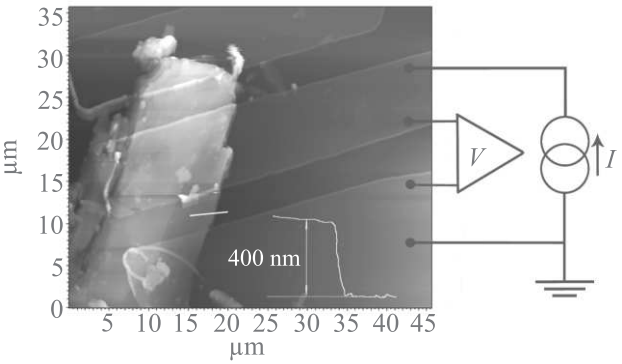

Fig. 1. (Color online) AFM image of the 400 nm thick sample with Au leads, evaporated over the WTe_2 flake. The leads are separated by 5 μm intervals. Inset demonstrates the AFM scan of the flake profile between the contact leads, along the white line in the image. Schematic diagram of the measurement circuit is also shown for the two-point connection scheme. For correct measurement of the low-resistance samples, we apply current I between the leads and measure the resulting voltage drop V. These measurements can be carried out in external electric field by applying gate voltage to the silicon wafer, separated from the flake by 300 nm SiO_2 layer. The measurements are performed at room temperature for WTe_2 samples of different thicknesses and lateral sizes, since ferroelectric domains have been previously observed in WTe_2 semimetal at room temperature [1]

To our surprise, we observe small but noticeable hysteresis in the experimental dV/dI with current sweep direction, so WTe_2 differential resistance is affected by the sign of the current change. Differential resistance $dV/dI(I)$ is a maximum at zero bias, it falls symmetri-

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cally at positive and negative currents by about 20 % in a full current range.

The hysteresis reflects some slow relaxation process in charge transport through WTe_2. To demonstrate the relaxation directly, we show $dV/dI(t)$ time-dependent curves, which are found to depend on the sign of the current change. We can estimate relaxation time as about 300 s. This behavior well correlates with the hysteresis in $dV/dI(I)$ curves. These effects are intrinsic to bulk WTe_2, which can be confirmed by measurements in a standard four-point connection scheme, where the Au-WTe_2 interfaces are excluded.

We can also study effect of the normal-to-the-plane electric field on $dV/dI(I)$ curves by using silicon substrate as a gate electrode. Increasing the gate voltage value shifts $dV/dI(I)$ curves down irrespective of the gate voltage sign, so the dV/dI level is in a maximum at zero gate voltage and falls symmetrically both to positive and negative gate voltage values, in contrast to the standard asymmetric accumulation/depletion field-effect transistor behavior.

The hysteresis amplitude can be demonstrated directly by subtracting two $dV/dI(I)$ curves for opposite current sweep directions at fixed gate voltage. The resulting $\Delta dV/dI(I)$ shows a maximum at the -1 mA negative current and a minimum at the $+1$ mA positive one. These results can be reproduced for samples of different thicknesses and lateral sizes, and, therefore, of different contact preparation techniques.

Even well-conducting WTe_2 single crystals demonstrate ferroelectricity at room temperature, which has been shown by direct visualization of ferroelectric domains [1]. The spontaneous polarization of these domains is normal to the WTe_2 layers, it can be affected by external electric field [1]. Due to the presence of the metallic conduction, there are two possible directions of the external electric fields in our setup: (i) gate field, $E_{\text{gate}} = V_g/d$, where $d = 300$ nm is the SiO_2 oxide thickness, E_g is directed normally to the WTe_2 surface; (ii) source-drain field $E_{sd} = \rho j$, which is connected with the flowing current, E_{sd} is parallel to the WTe_2 surface. The achievable values of the fields ($\sim 10^4$–10^6 V/m) are too small to align polarization of the whole WTe_2 flake, so they mostly affect the domain wall regions. Due to the field direction, E_{gate} moves the position of the wall, while E_{sd} changes the wall region width. Thus, any variation of electric fields leads to the additional polarization current. The latter we observe as slow relaxation in dV/dI, since polarization current is connected with lattice deformation in ferroelectrics. The possibility to induce polarization current by source-drain field variation is unique for WTe_2, since it is a direct consequence of ferroelectricity and metallic conductivity coexistence [1].

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